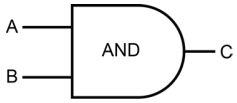
Exercise 1: AND/NAND Logic Functions

EXERCISE OBJECTIVE

When you have completed this exercise, you will be able to determine the operation of an AND and a NAND logic gate. You will verify your results by generating truth tables for each function.

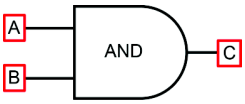
EXERCISE DISCUSSION

The schematic symbol of a two-input AND gate and the Boolean equation for the AND gate are shown here.



C = A•B

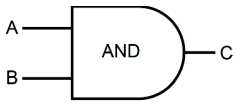
Input signals are labeled A and B, and the output is labeled C.



C = A•B

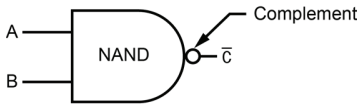
The Boolean equation for the AND gate states that C is high when A and B are high. The AND operation is indicated by the dot between A and B.

NOTE: A•B and AB without the "•" are identical.



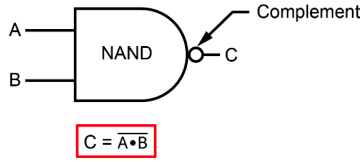
C = A•B

The schematic symbol of a two-input NAND gate and the Boolean equation for the NAND gate are shown here.

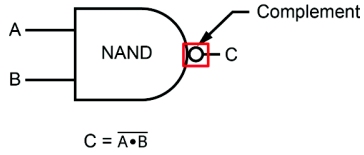


$\overline{C}$ = A•B

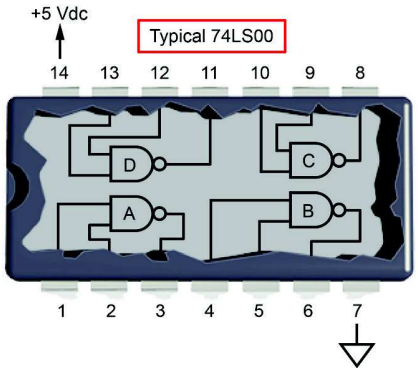
The Boolean equation for the NAND gate states that C is low when A and B are high. The bar over A·B represents the complement.



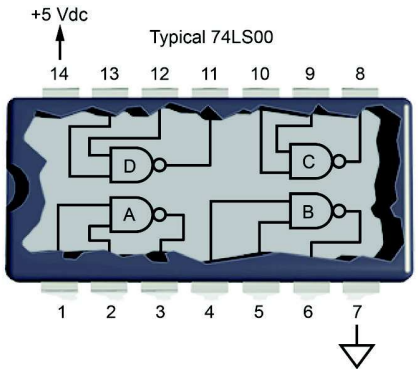
The NAND gate function has a bubble drawn at the output side of the gate. The bubble indicates a complement.



Below is the pin-out configuration for the 74LS00 NAND, SSI IC used in this exercise.

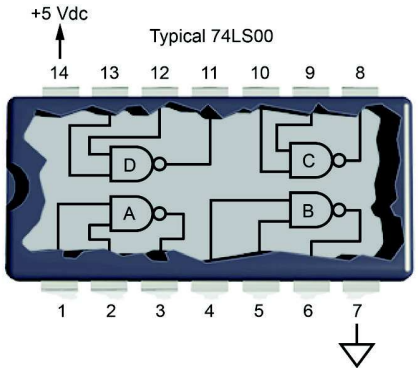


Pins 14 and 7 supply power to the IC. The IC provides four separate two-input NAND gates labeled A through D.



Pin 11 is the output for which gate?

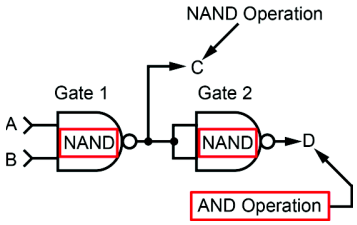
a. A
b. B
c. C
d. D



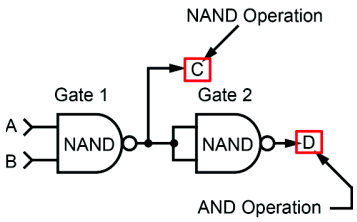
For the 74LS00 IC, inputs may be tied to other inputs, or outputs may be connected to inputs; however, outputs cannot be connected to one another.

Unused inputs generally are pulled high (connected to 5 Vdc) through a pull-up resistor.

Two NAND gates can be cascaded (connected in series) to generate an AND operation, as shown.



Output C provides a NAND response to circuit inputs A and B. Output C is complemented by the action of GATE 2. In turn, this gate generates an AND operation for circuit inputs A and B at output D.



This is the truth table for the circuit.

Inputs		Outputs	
		NAND	AND
A	B	C	D
1	1	0	1
1	0	1	0
0	1	1	0
0	0	1	0

Complements

Outputs C and D are complements. Output column C provides the NAND function truth table, while output column D provides the AND function truth table.

Inputs		Outputs	
		NAND	AND
A	B	C	D
1	1	0	1
1	0	1	0
0	1	1	0
0	0	1	0

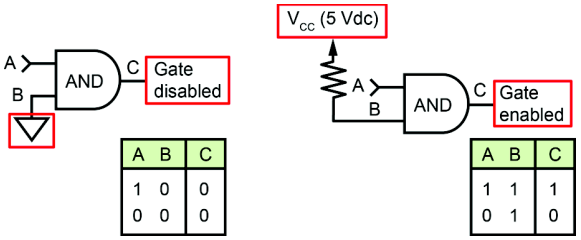
Complements

A and B are the two circuit inputs. Four unique input conditions test all possible input combinations.

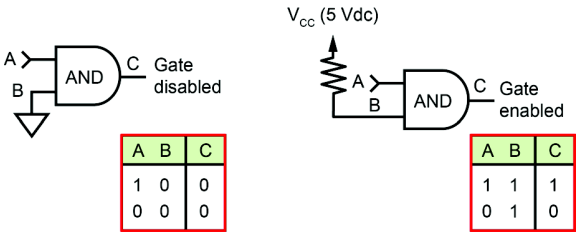
Inputs		Outputs	
		NAND	AND
A	B	C	D
1	1	0	1
1	0	1	0
0	1	1	0
0	0	1	0

Complements

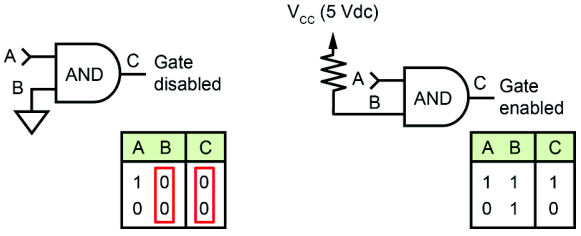
A low logic state at any input disables an AND gate. A high logic state at one input of a two-input AND gate enables the gate.



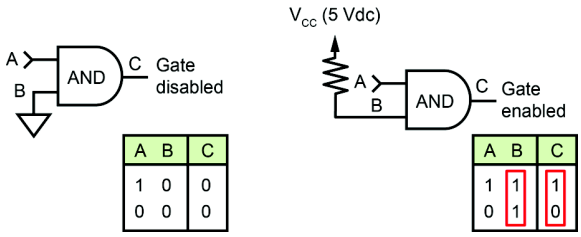
The disable and enable combinations and the truth tables for an AND gate are shown here.



If one input is held low, the output is always low and the gate is disabled.



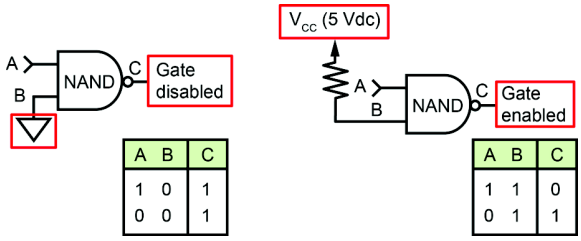
If one input is held high, the output is the same level as the other input and the gate is enabled.



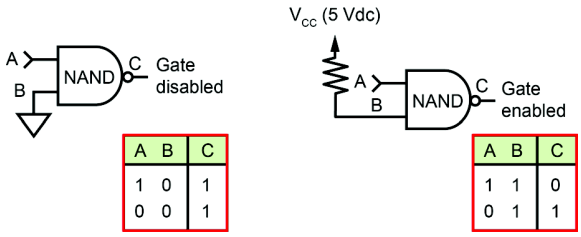
If you wanted to disable an AND gate, you would pull one input

a. high.
b. low.

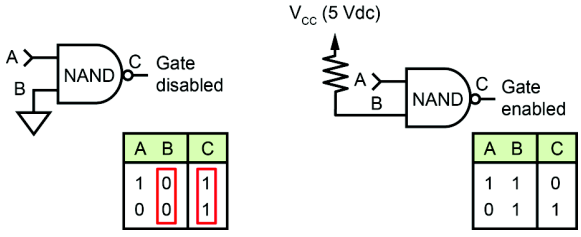
A low level at any input disables a NAND gate. A high level at one input of a NAND gate enables the gate.



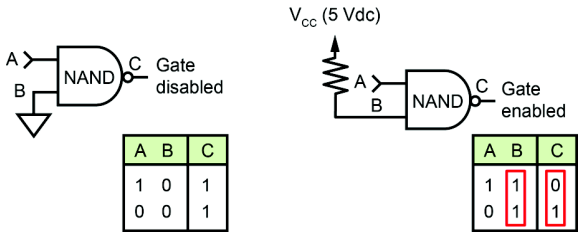
The disable and enable combinations and the truth tables for a NAND gate are shown here.



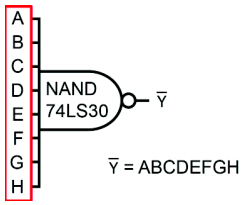
A disabled NAND gate locks out its other input and generates a high level (1) output, as shown in the truth table.



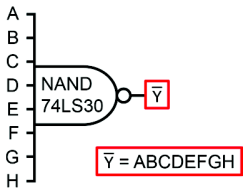
An enabled NAND gate complements the other input, as shown in the truth table.



An eight-input NAND gate (74LS30) is shown. The operating principles of a two-input NAND gate apply to gates having more than two inputs.



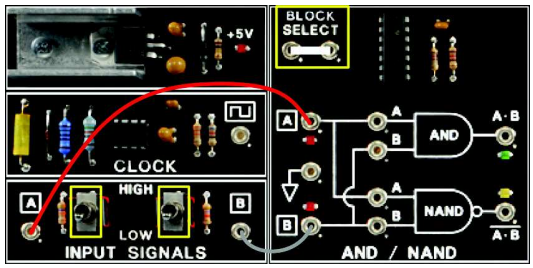
The output of this gate is low only when all inputs are high. Any one input at a low level locks out the other inputs (the output is always high).



PROCEDURE

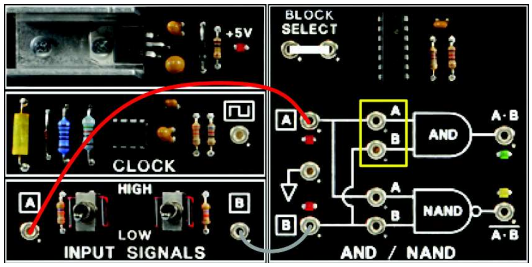
☐ 1. Locate the AND/NAND circuit block, and connect the circuit shown. Activate BLOCK SELECT. Place both toggle switches in the LOW position.

NOTE: A high logic level turns on an LED. You can verify the state of a signal, as indicated by a circuit LED, by connecting your multimeter to the appropriate test point.



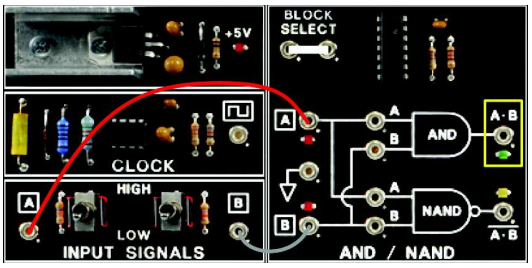
2. What are the logic levels at AND gate inputs A and B?

a. both low
b. both high



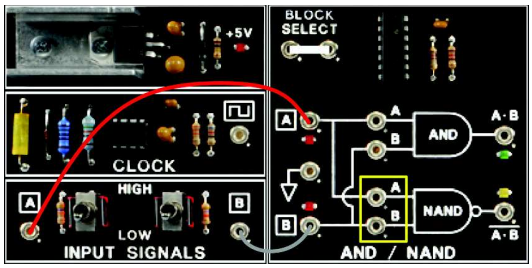
3. Based on the input levels, what is the AND gate output level?

a. 1
b. 0



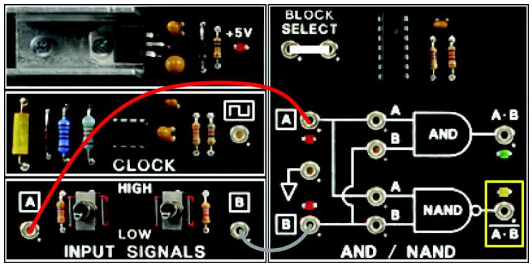
4. What are the logic levels at the NAND gate inputs?

a. both low
b. both high



5. What is the logic level at the output of the NAND gate?

a. 1
b. 0



6. The table shows the AND and NAND outputs when inputs A and B are low.

Inputs		Outputs	
		AND	NAND
A	B	A • B	$\overline{A \bullet B}$
0	0	0	1

7. Place toggle switch A in the HIGH position. What is the AND gate output?

a. 1
b. 0

Inputs		Outputs	
		AND	NAND
A	B	A • B	$\overline{A \bullet B}$
0 1	0 0	0 ?	1

8. What is the NAND gate output?

a. 1
b. 0

Inputs		Outputs	
		AND	NAND
A	B	A • B	$\overline{A \bullet B}$
0 1	0 0	0 0	1 ?

9. Place toggle switch A in the LOW position and switch B in the HIGH position. What is the AND gate output?

a. 1
b. 0

Inputs		Outputs	
		AND	NAND
A	B	A • B	$\overline{A \bullet B}$
0 1 0	0 0 1	0 0 ?	1 1

10. What is the output of the NAND gate?

a. 1
b. 0

Inputs		Outputs	
		AND	NAND
A	B	A • B	$\overline{A \bullet B}$
0 1 0	0 0 1	0 0 0	1 1 ?

11. Set both switches A and B high. What is the AND output?
    a. 1
    b. 0

Inputs		Outputs	
		AND	NAND
A	B	A • B	$\overline{A \cdot B}$
0	0	0	1
1	0	0	1
0	1	0	1
1	1	?	

12. What is the NAND gate output?
    a. 1
    b. 0

Inputs		Outputs	
		AND	NAND
A	B	A • B	$\overline{A \cdot B}$
0	0	0	1
1	0	0	1
0	1	0	1
1	1	1	?

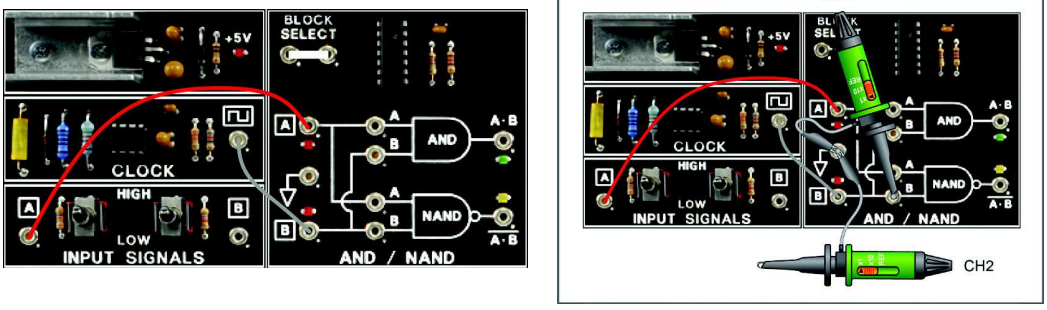
13. Based on the truth table, when is the AND gate output high?
    a. when any input is high
    b. when both inputs are high

Inputs		Outputs	
		AND	NAND
A	B	A • B	$\overline{A \cdot B}$
0	0	0	1
1	0	0	1
0	1	0	1
1	1	1	0

14. Based on the truth table, are the outputs of the AND and NAND gates complementary?
    a. yes
    b. no

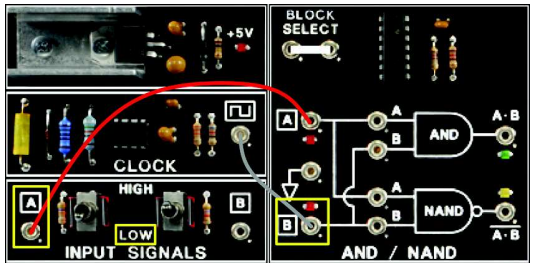
Inputs		Outputs	
		AND	NAND
A	B	A • B	$\overline{A \cdot B}$
0	0	0	1
1	0	0	1
0	1	0	1
1	1	1	0

15. Connect the circuit shown here. Connect channel 1 of your oscilloscope to circuit input B. Use channel 2 to monitor other circuit points as required.



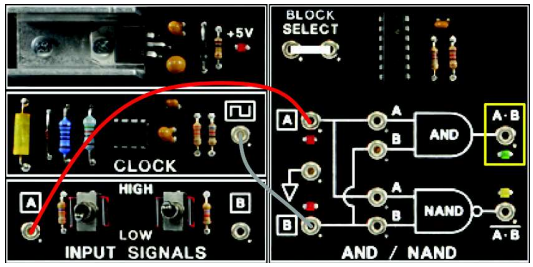
NOTE: LEDs will appear to be constantly on due to the pulse train input signal. This action does not alter the expected circuit operation. You may disable the circuit block LEDs by removing BLOCK SELECT.

16. Place switch A in the LOW position. Circuit input signal B is a square wave pulse train as seen on oscilloscope channel 1.

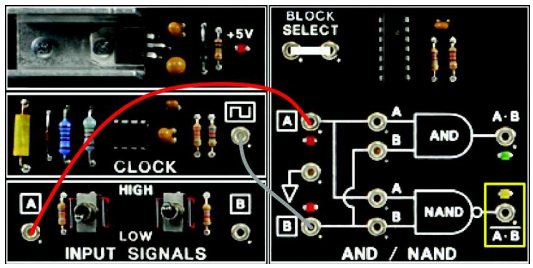


17. Monitor the AND gate and NAND gate outputs on channel 2 of the scope. Are the gates enabled or disabled?
    a. enabled
    b. disabled

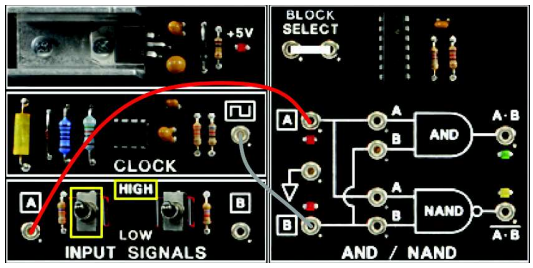
18. Is the AND gate output high or low?
    a. high
    b. low



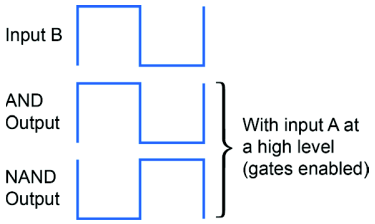
19. Is the NAND gate output high or low?
    a. high
    b. low



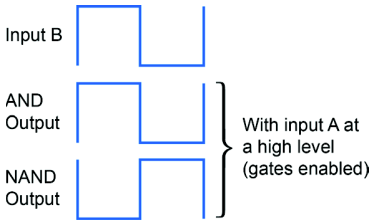
20. Place switch A in the HIGH position. Monitor the output of each gate. Are the gates enabled or disabled by the high input at A?
    a. enabled
    b. disabled



21. Refer to the waves shown here, and compare the circuit outputs with the circuit input. With respect to input signal B, the AND output is
    a. in phase.
    b. out of phase.



22. With respect to input signal B, the NAND gate output is
    a. in phase.
    b. out of phase.

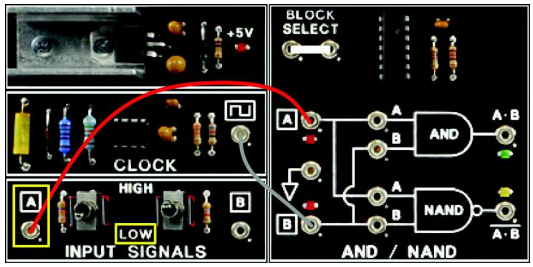


CONCLUSION

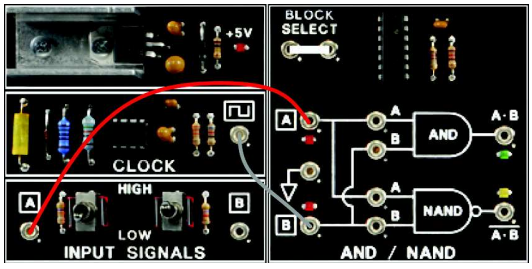
- The output of an AND gate is high only when all inputs are high.
- The output of a NAND gate is low only when all inputs are high.
- A low input disables an AND or a NAND gate.
- A high input (two-input gate) will enable an AND or a NAND gate.
- The output of an enabled AND gate is in phase with its input.
- The output of an enabled NAND gate is the complement of its input.

REVIEW QUESTIONS

1. Locate the AND/NAND circuit block and connect the circuit shown. Disable the circuit gates by placing toggle switch A in the LOW position.



   Place CM switch 6 in the ON position. The CM
   a. enables the NAND gate but not the AND gate.
   b. disables the clock signal at input B.
   c. enables the AND and NAND gates.
   d. causes the AND and NAND gate outputs to be in phase.

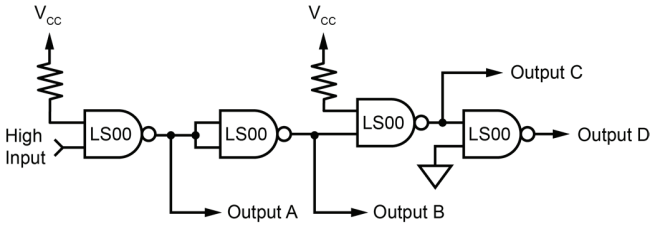


2. Place CM switch 7 in the ON position. The CM
   a. places a logic 1 signal at input B to the gates.
   b. prevents the gates from responding to changes at input A.
   c. enables the AND gate but disables the NAND gate.
   d. enables the NAND gate but disables the AND gate.

3. The output of an AND gate is high
   a. all of the time.
   b. when any input is low.
   c. when any input is high.
   d. when all inputs are high.

4. The output of a NAND gate is low
   a. all of the time.
   b. when any input is low.
   c. when any input is high.
   d. when all inputs are high.

5. In the circuit shown, output levels A through D are, respectively,
   a. low, high, low, and low.
   b. low, high, low, and high.
   c. high, low, low, and low.
   d. disabled due to the circuit pull-ups and to a common connection on the last gate.



NOTE: Make sure all CMs are cleared (turned off) before proceeding to the next section.